FIG. 1

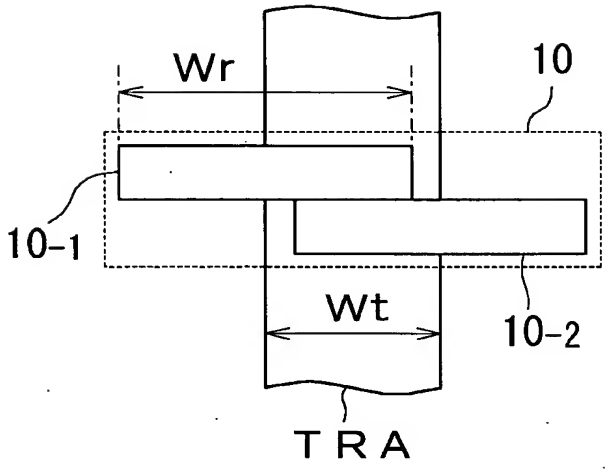

Wr
10
10-1
Wt
10-2
TRA

FIG. 6

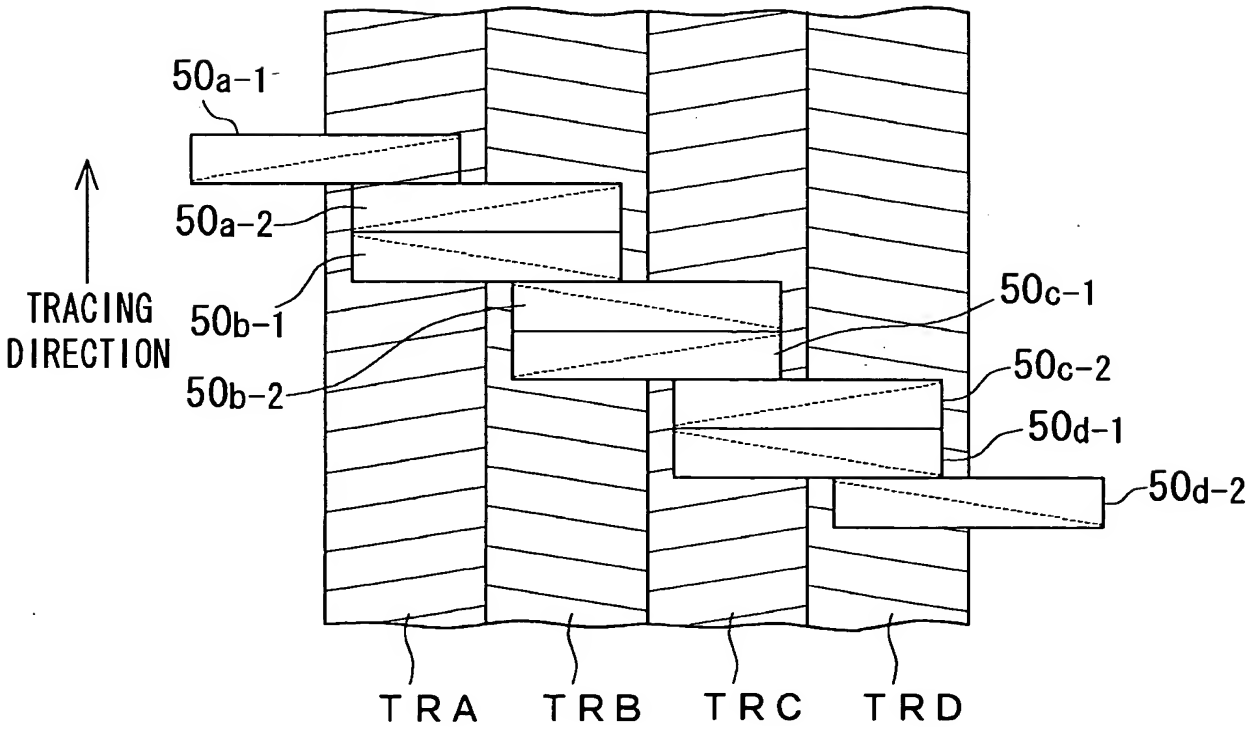

50a-1
50a-2
TRACING DIRECTION
50b-1
50b-2
50c-1
50c-2
50d-1
50d-2
TRA
TRB
TRC
TRD

FIG. 2A

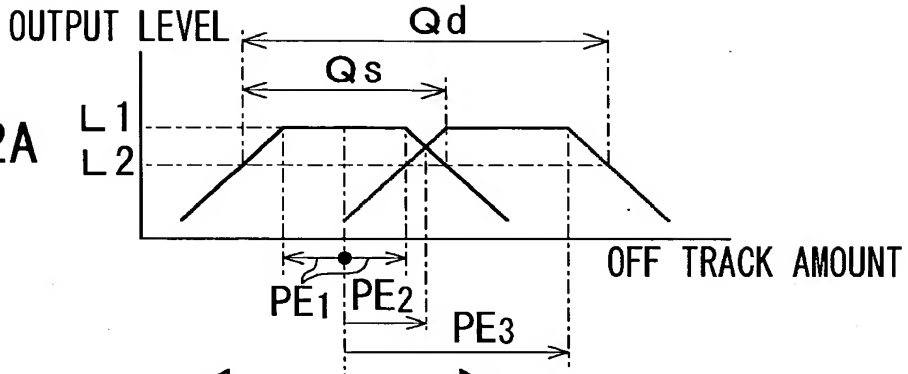


FIG. 2B

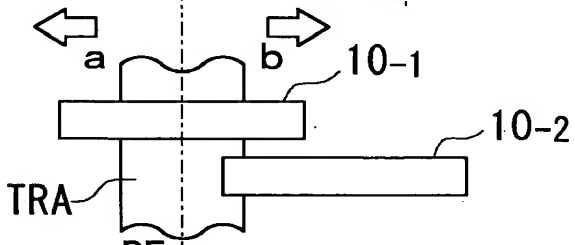


FIG. 2C

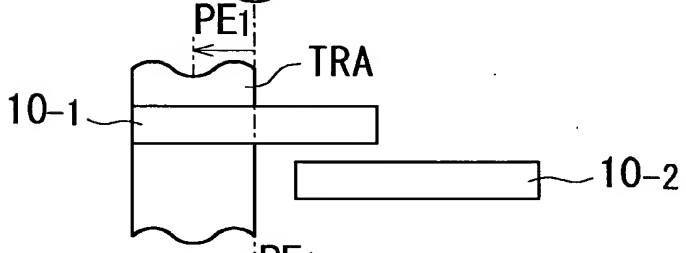


FIG. 2D

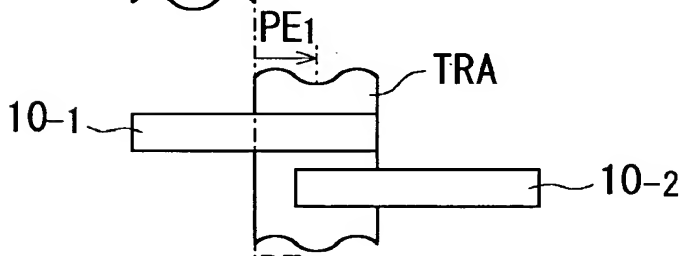


FIG. 2E

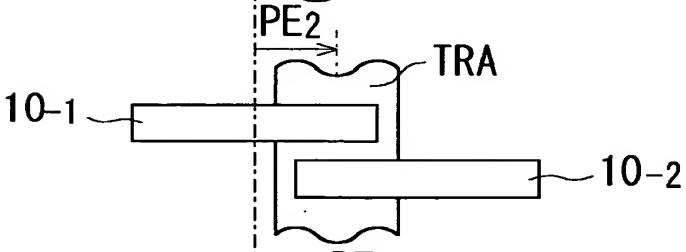
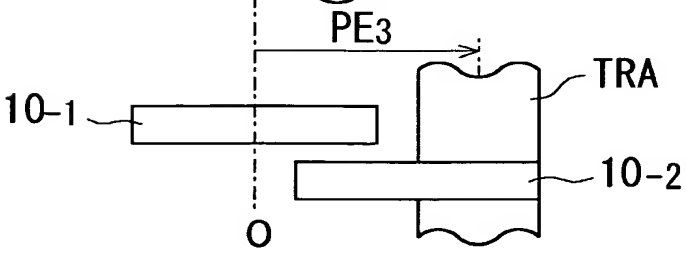


FIG. 2F



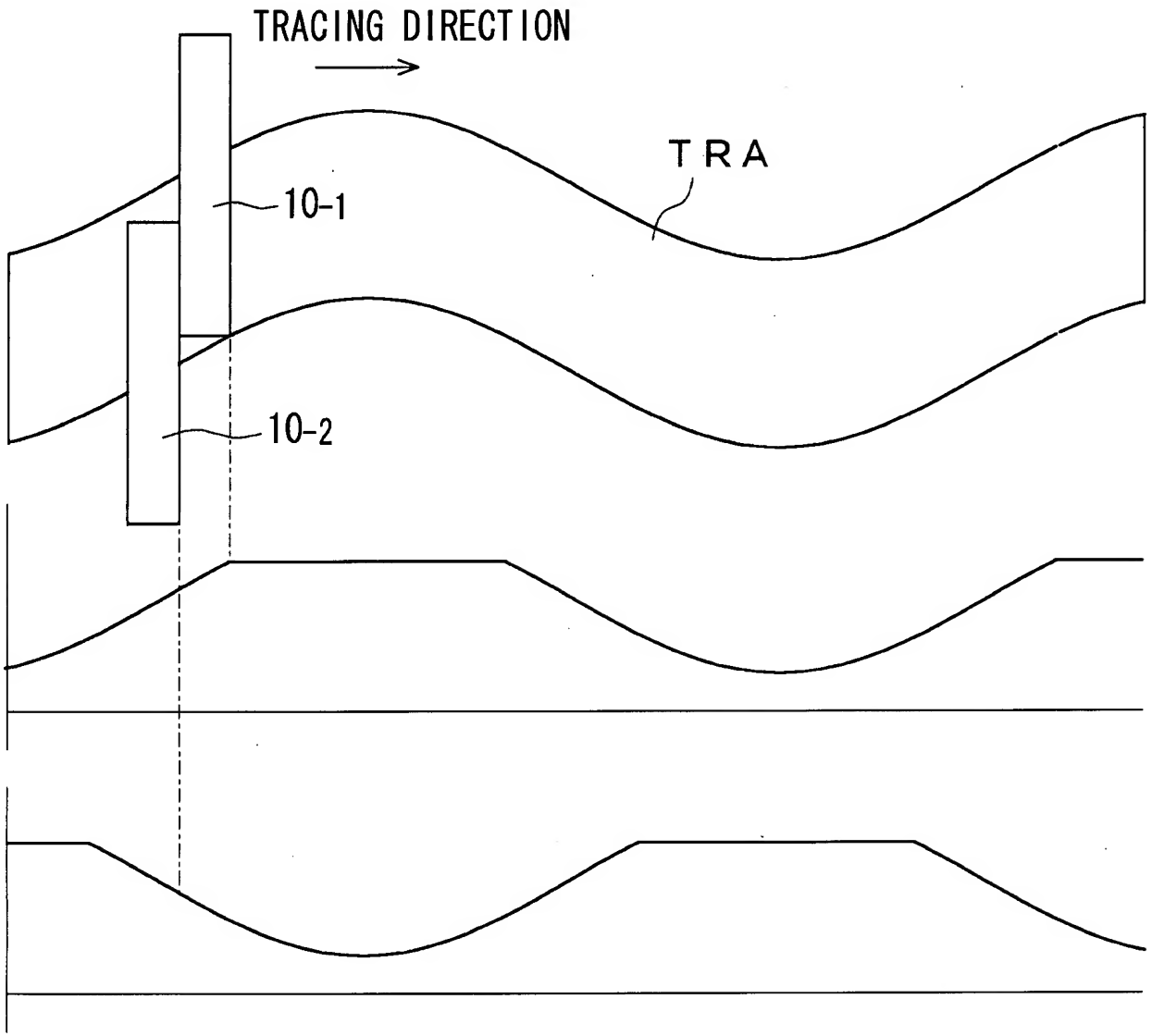


FIG. 3A

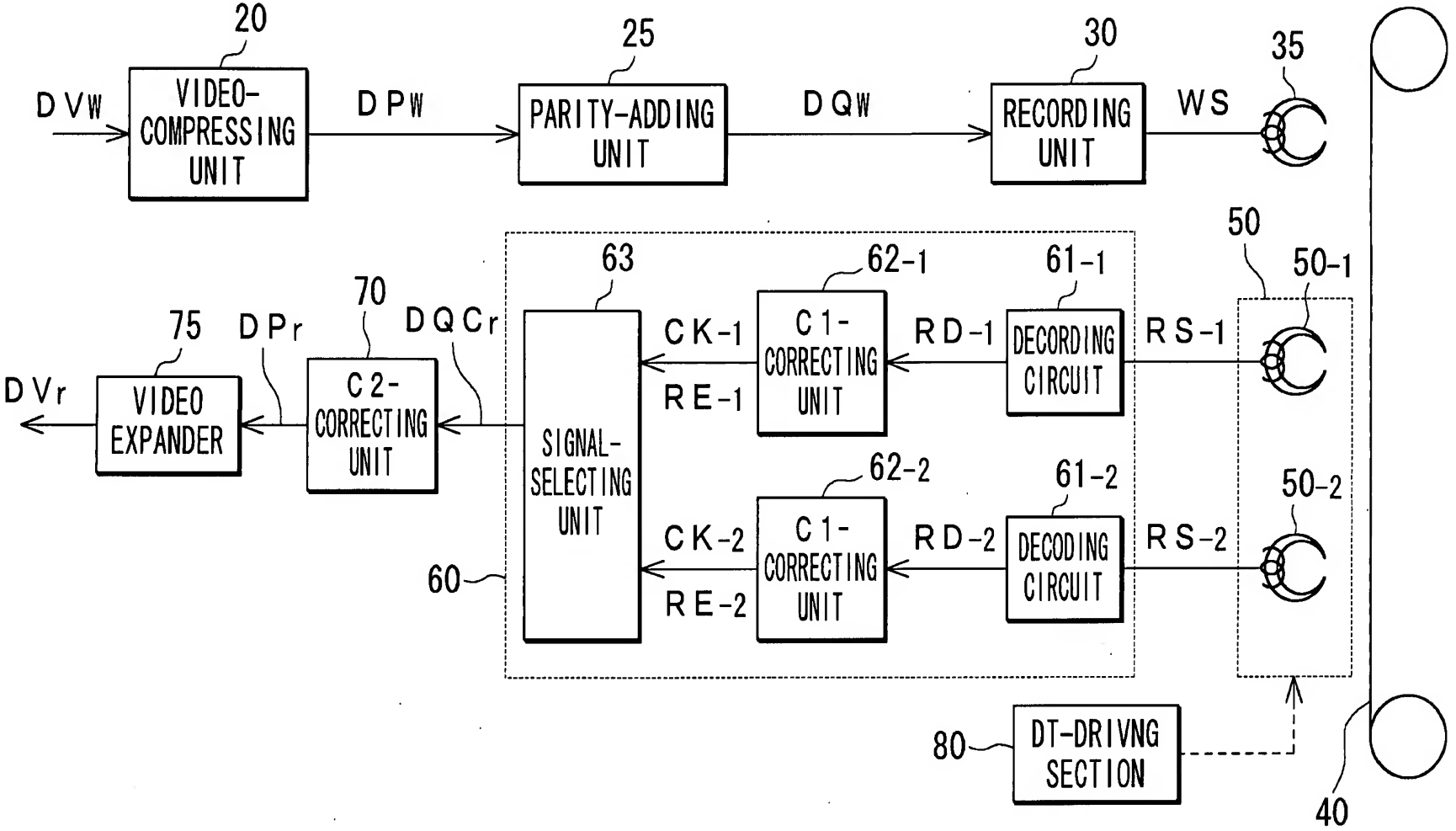
FIG. 3B

OUTPUT LEVEL OF REPRODUCING HEAD 10-1

FIG. 3C

OUTPUT LEVEL OF REPRODUCING HEAD 10-2

FIG. 4


20
VIDEO-COMPRESSING UNIT
DVW
DPW
25
PARITY-ADDING UNIT
DQW
30
RECORDING UNIT
WS
35
50
50-1
63
62-1
61-1
70
75
DPr
DQCr
CK-1
C1-CORRECTING UNIT
RD-1
DECORDING CIRCUIT
RS-1
RE-1
DVr
VIDEO EXPANDER
C2-CORRECTING UNIT
SIGNAL-SELECTING UNIT
62-2
61-2
50-2
CK-2
C1-CORRECTING UNIT
RD-2
DECODING CIRCUIT
RS-2
RE-2
60
80
DT-DRIVNG SECTION
40

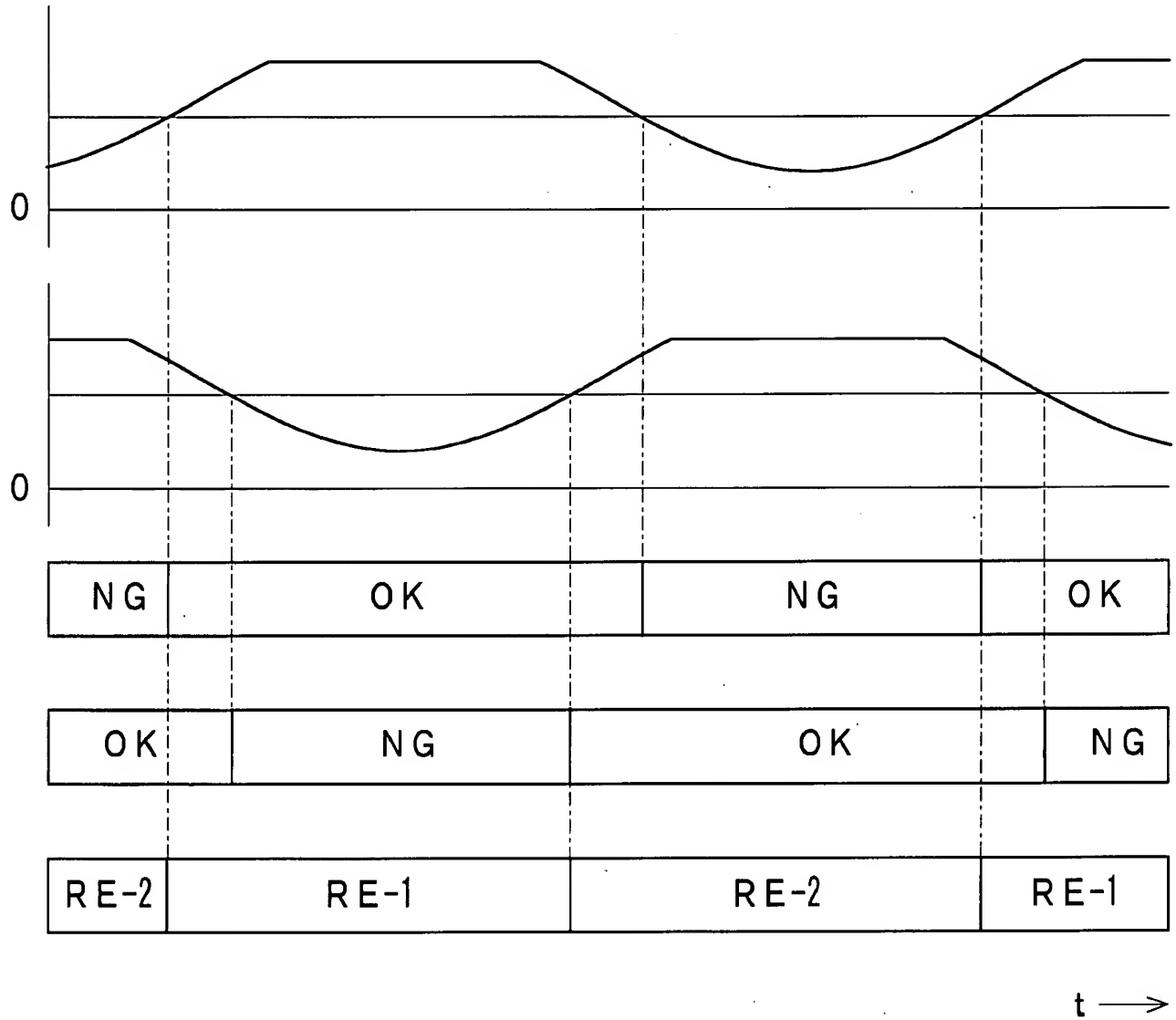


FIG. 5A
OUTPUT LEVEL OF REPRODUCING HEAD 50-1

FIG. 5B
OUTPUT LEVEL OF REPRODUCING HEAD 50-2

FIG. 5C
(CK-1)

FIG. 5D
(CK-2)

FIG. 5E
(DQCr)

FIG. 7A

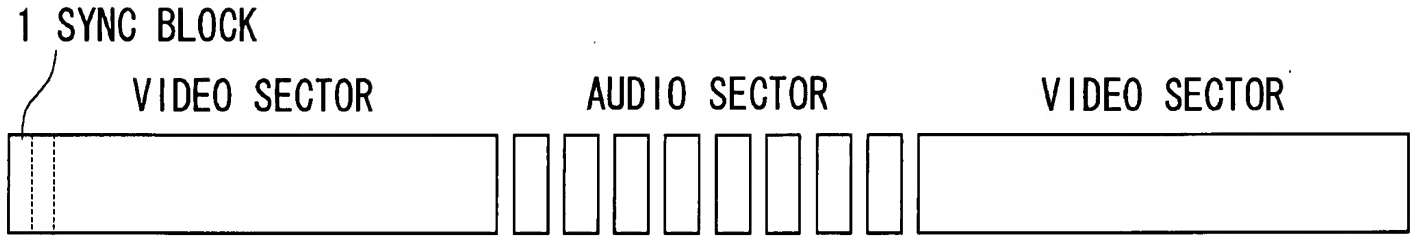
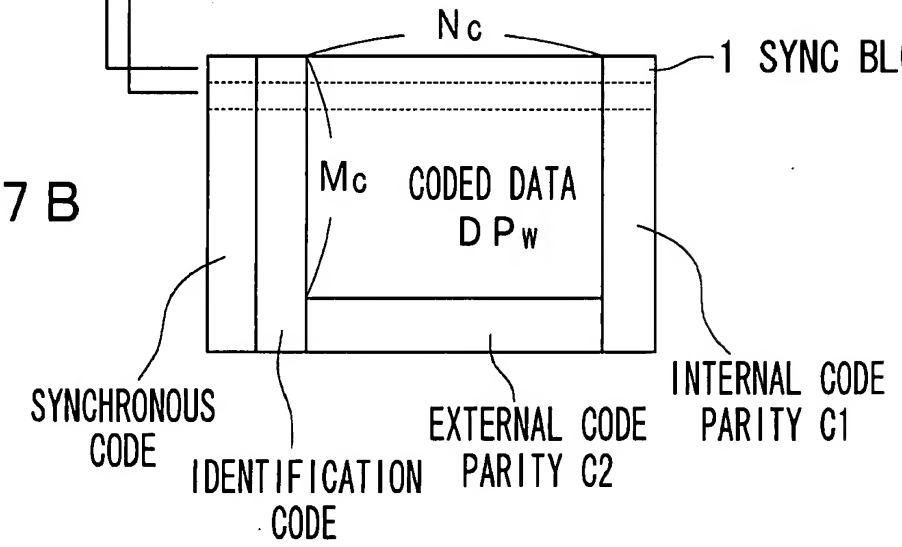

1 SYNC BLOCK
VIDEO SECTOR
AUDIO SECTOR
VIDEO SECTOR

FIG. 7B


Nc
1 SYNC BLOCK
Mc
CODED DATA
DPw
SYNCHRONOUS CODE
IDENTIFICATION CODE
EXTERNAL CODE PARITY C2
INTERNAL CODE PARITY C1

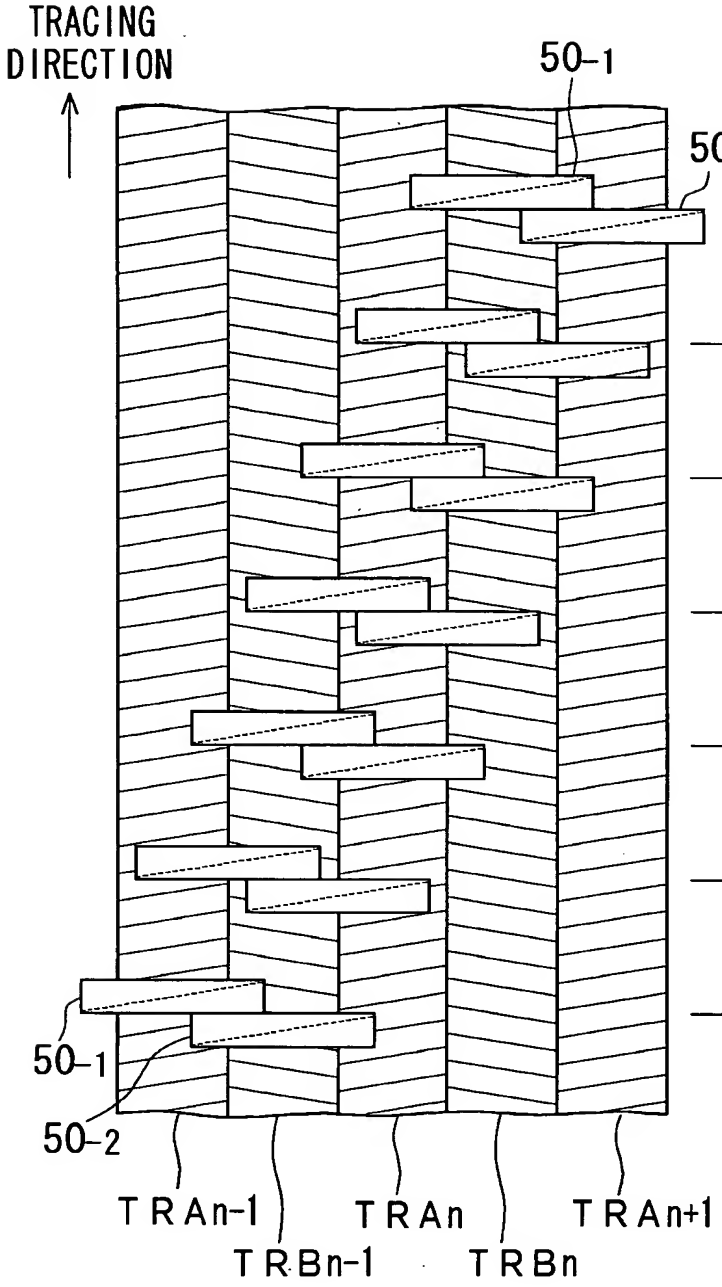
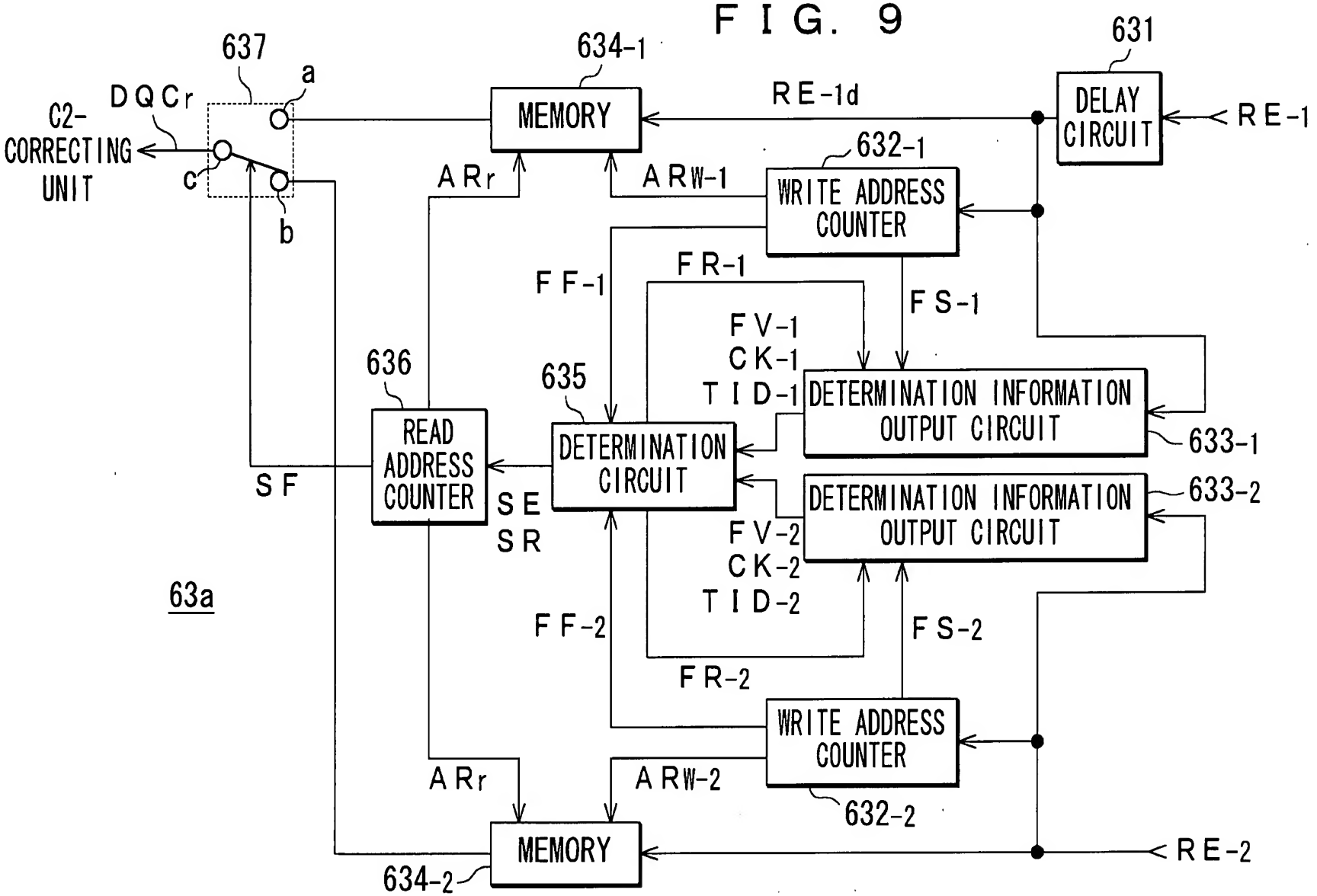


FIG. 8A

STATE	TRACK IDENTIFICATION INFORMATION TID-1	TRACK IDENTIFICATION INFORMATION TID-2
1	EROOR	TRAn+1
2	TRAn	TRAn+1
3	TRAn	ERROR
4	TRAn	TRAn
5	ERROR	TRAn
6	TRAn-1	TRAn
7	TRAn-1	ERROR

FIG. 8B

FIG. 9


637
a
DQCr
C2-
CORRECTING
UNIT
c
b
634-1
MEMORY
RE-1d
631
DELAY
CIRCUIT
RE-1
632-1
WRITE ADDRESS
COUNTER
ARr
ARW-1
FF-1
FR-1
FS-1
FV-1
CK-1
TID-1
636
635
READ
ADDRESS
COUNTER
DETERMINATION
CIRCUIT
DETERMINATION INFORMATION
OUTPUT CIRCUIT
633-1
633-2
SF
SE
SR
FV-2
CK-2
TID-2
63a
FF-2
FS-2
FR-2
WRITE ADDRESS
COUNTER
ARr
ARW-2
632-2
MEMORY
RE-2
634-2

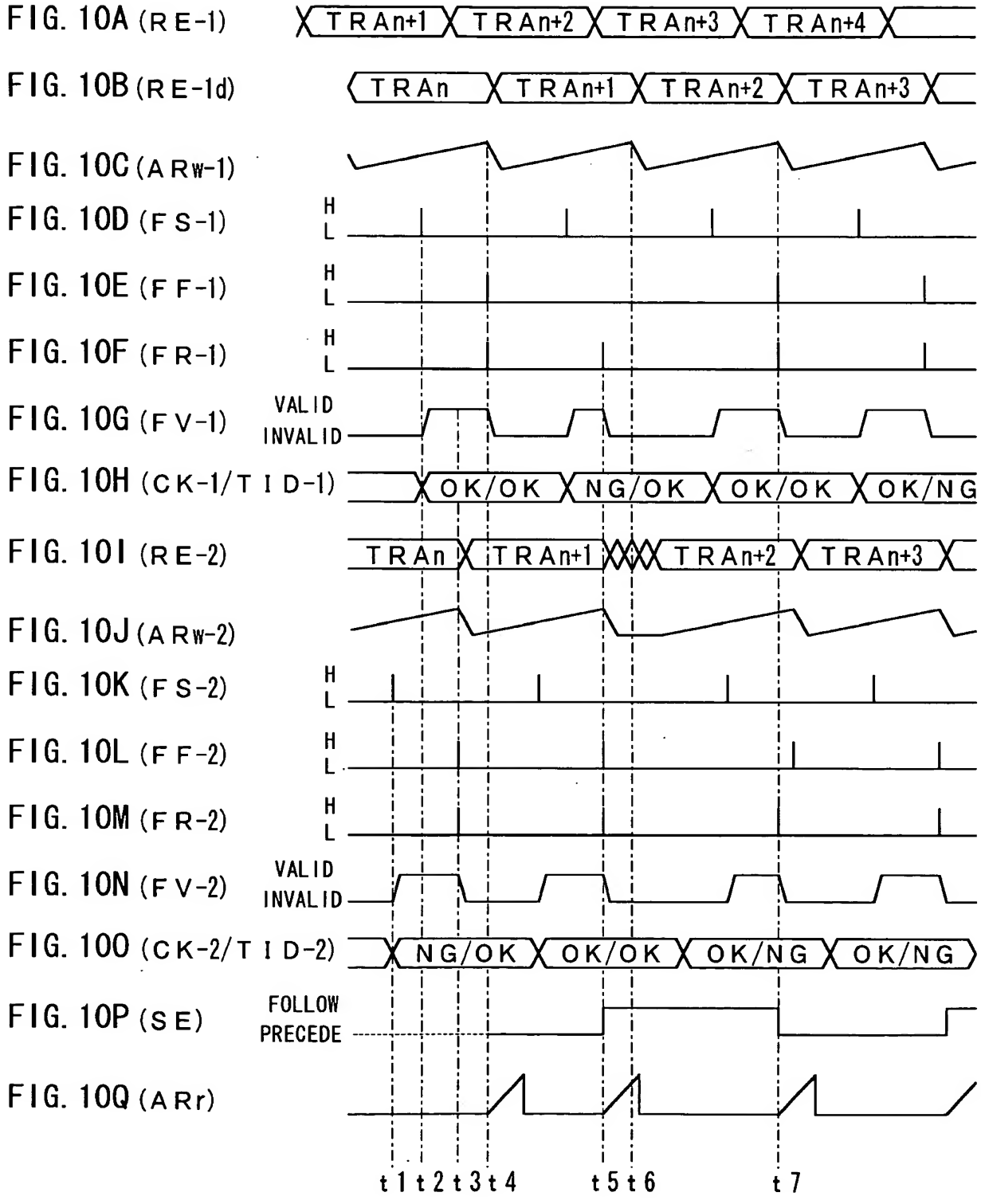


FIG. 10A (RE-1)
TRAn+1
TRAn+2
TRAn+3
TRAn+4
FIG. 10B (RE-1d)
TRAn
TRAn+1
TRAn+2
TRAn+3
FIG. 10C (ARw-1)
FIG. 10D (FS-1)
H
L
FIG. 10E (FF-1)
H
L
FIG. 10F (FR-1)
H
L
FIG. 10G (FV-1)
VALID
INVALID
FIG. 10H (CK-1/TID-1)
OK/OK
NG/OK
OK/OK
OK/NG
FIG. 10I (RE-2)
TRAn
TRAn+1
TRAn+2
TRAn+3
FIG. 10J (ARw-2)
FIG. 10K (FS-2)
H
L
FIG. 10L (FF-2)
H
L
FIG. 10M (FR-2)
H
L
FIG. 10N (FV-2)
VALID
INVALID
FIG. 10O (CK-2/TID-2)
NG/OK
OK/OK
OK/NG
OK/NG
FIG. 10P (SE)
FOLLOW
PRECEDE
FIG. 10Q (ARr)
t1 t2 t3 t4 t5 t6 t7

CONDITION NO.

FIG. 11

	INPUT								OUTPUT		
	FF-1	FF-2	FV-1	FV-2	CK-1	CK-2	TID-1	TID-2	SE	FR-1	FR-2
1	0	0	*	*	*	*	*	*	NOP	0	0
2	1	0	0	*	*	*	*	*	NOP	0	0
3	0	1	*	0	*	*	*	*	NOP	0	0
4	1	1	0	0	*	*	*	*	NOP	0	0
5	1	*	1	0	*	*	*	*	PRECEDE	1	0
6	1	*	1	1	OK	NG	*	*	PRECEDE	1	1
7	1	*	1	1	OK	OK	OK	*	PRECEDE	1	1
8	1	*	1	1	OK	OK	NG	NG	PRECEDE	1	1
9	1	0	1	1	OK	OK	NG	OK	NOP	1	0
10	1	1	1	1	OK	OK	NG	OK	FOLLOW	1	1
11	1	*	1	1	NG	NG	OK	*	PRECEDE	1	1
12	1	*	1	1	NG	NG	NG	NG	PRECEDE	1	1
13	1	0	1	1	NG	NG	NG	OK	NOP	1	1
14	1	1	1	1	NG	NG	NG	OK	FOLLOW	1	1
15	1	0	1	1	NG	OK	*	*	NOP	1	0
16	1	1	1	1	NG	OK	*	*	FOLLOW	1	1
17	0	1	0	1	*	*	*	*	FOLLOW	0	1
18	0	1	1	1	NG	OK	*	*	FOLLOW	1	1
19	0	1	1	1	OK	OK	NG	OK	FOLLOW	1	1
20	0	1	1	1	OK	OK	OK	*	NOP	0	1
21	0	1	1	1	OK	OK	NG	NG	NOP	0	1
22	0	1	1	1	NG	NG	NG	OK	FOLLOW	1	1
23	0	1	1	1	NG	NG	OK	*	NOP	0	1
24	0	1	1	1	NG	NG	NG	NG	NOP	0	1
25	0	1	1	1	OK	NG	*	*	NOP	0	1